UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/051,263	08/07/1998	GEORGE W. SHAW	NANO-002/01U	7818

40972 7590 12/27/2006
HENNEMAN & ASSOCIATES, PLC
714 W. MICHIGAN AVENUE
THREE RIVERS, MI 49093

EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/27/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/051,263	SHAW ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 27-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 27-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 April 1998* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/7/98; 5/23/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12 and 27-30 have been considered. Claims 13-26 and 31-44 were not considered, since they were not part of the elected group.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Extension of Time for 1 Month as received on 25 September 2006 and Amendment as received 25 September 2006.

Election/Restrictions

3. Applicant's election of claims 1-12 and 27-30 in the reply filed on 25 September is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Priority

4. Acknowledgment is made of applicant's claim for priority under 35 U.S.C. 371.

Information Disclosure Statement

5. The information disclosure statement (IDS) submitted on 23 May 2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

6. The information disclosure statement filed 07 August 1998 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information

referred to therein has not been considered. The Examiner could not locate copies of the non-patent literature, therefore, they were not considered.

Specification

7. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

8. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

9. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings contain handwritten identifiers that, at times, are hard to distinguish.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 1-12 and 27-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. Claims 1-12 and 27-30 recite the limitation "said central processing unit". There is insufficient antecedent basis for this limitation in the claim. A central processing unit has not been previously established in the claim.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 1-2, 4-12, and 27-30 are rejected under 35 U.S.C. 102(b) as being taught by Briggs et al., U.S. Patent Number 4,649,471 (herein referred to as '471) and U.S. Patent Number 4,626,985 (herein referred to as '985). '985 was incorporated by reference into '471 in column 3, lines 60-63.

15. Examiner notes that for purposes of the rejection the recitations "said central processing unit" in the claim is assumed to be the same as the microprocessing unit.

16. Referring to claim 1, '471 and '985 have taught a microprocessor system, comprising

a. A microprocessing unit ('471 column 2, lines 4-45; column 2, line 57 to column 3, line 27; Figure 2A; and Figure 2B),

b. An input-output processor (IOP) ('471 column 2, lines 4-45; column 2, line 57 to column 3, line 27; Figure 2A; and Figure 2B),

c. A global memory unit coupled to said central processing unit and to said IOP ('471 column 2, lines 4-45; column 2, line 57 to column 3, line 27; Figure 2A; and Figure 2B), and

d. Means for arbitrating access of said central processing unit and said IOP to said global memory unit ('471 column 3, line 37 to column 4, line 52; column 5, lines 43-59; and Figure 3). In regards to '471, the focus of the discussion was on the bus arbitration, but there is some discussion regarding indications showing which

memory is being accessed and which device is accessing it. Also, the bus arbitration does affect which device accesses the global memory, since it controls which devices uses the bus to transmit data to its destination.

17. Referring to claim 2, '471 and '985 have taught the microprocessor system of claim 1 in which said global memory unit comprises a plurality of global registers ('471 column 2, lines 4-45). In regards to '471, '471 mentions in column 2, lines 24-25 that there are not only I/O devices but also registers that as part of the system and mapped in memory space.

18. Referring to claim 4, '471 and '985 have taught the microprocessor system of claim 1 further including a memory interface unit coupled to said global memory unit, to said microprocessing unit, and to said IOP ('471 column 3, lines 44-66). In regards to '471, the address decoder, which determines which memory address is being accessed by the CPU or IOP, is the memory interface.

19. Referring to claim 5, '471 and '985 have taught the microprocessor system of claim 4 further including a means for arbitrating access of said memory interface unit and said microprocessing unit to said global memory unit ('471 column 3, line 37 to column 4, line 52; column 5, lines 43-59; and Figure 3). In regards to '471, the focus of the discussion was on the bus arbitration, but there is some discussion regarding indications showing which memory is being accessed and which device is accessing it. Also, the bus arbitration does affect which device accesses the global memory, since it controls which devices uses the bus to transmit data to its destination and affects which memory address is accessing what address.

20. Referring to claim 6, '471 and '985 have taught the microprocessor system of claim 5 additionally comprising a system memory and at least one input-output device coupled to said

memory interface unit and wherein each storage location in said global memory unit holds a single address comprised of a first grouping of address bits coupled to address said system memory and a second grouping of address bits coupled to address said at least one input-output device ('471 column 3, line 44 to column 4, line 19 and Figure 3).

21. Referring to claim 7, '471 and '985 have taught the microprocessor system of claim 5 additionally comprising a system memory, at least one input-output device and a system bus coupled to said memory interface unit, said system bus having a first grouping of address lines coupled to address said-system memory and a second grouping of address lines coupled to address said at least one input-output device ('471 column 3, line 44 to column 4, line 19 and Figure 3).

22. Referring to claim 8, '471 and '985 have taught a microprocessor system, comprising

a. A microprocessing unit ('471 column 2, lines 4-45; column 2, line 57 to column 3, line 27; Figure 2A; and Figure 2B),

b. An input-output processor (IOP) ('471 column 2, lines 4-45; column 2, line 57 to column 3, line 27; Figure 2A; and Figure 2B),

c. A memory interface unit through which said central processing unit and said IOP are selectively coupled to a system bus ('471 column 3, lines 44-66). In regards to '471, the address decoder, which determines which memory address is being accessed by the CPU or IOP, is the memory interface, and

d. Means for granting said IOP access to said system bus at predetermined intervals ('471 column 3, line 37 to column 4, line 52; column 5, lines 43-59; and Figure 3; and '985 column 4, line 21 to column 5, line 25 and Figure 4). In regards to '471,

the focus of the discussion was on the bus arbitration and '985 discuses the timing of the accesses allowed to the bus.

23. Referring to claim 9, '471 and '985 has taught the microprocessor system of claim 8 wherein said memory interface unit includes means for defining available time slots during which said system bus may be accessed, said available time slots being defined as being between accesses to said system bus by said IOP at said predetermined intervals ('471 column 3, line 37 to column 4, line 52; column 5, lines 43-59; and Figure 3; and '985 column 4, line 21 to column 5, line 25 and Figure 4).

24. Referring to claim 10, '471 and '985 has taught the microprocessor system of claim 8 wherein said memory interface unit includes means for computing a bus access time required for one or more bus cycles involving said system bus, and for allocating one of said available time slots equal to or longer than said access time for execution of said one or more bus cycles ('471 column 3, line 37 to column 4, line 52; column 5, lines 43-59; and Figure 3; and '985 column 4, line 21 to column 5, line 25 and Figure 4).

25. Referring to claim 11, '471 and '985 has taught the microprocessor system of claim 10 wherein said one or more bus cycles are memory cycles ('471 column 3, line 37 to column 4, line 52; column 5, lines 43-59; and Figure 3; and '985 column 4, line 21 to column 5, line 25 and Figure 4).

26. Referring to claim 12, '471 and '985 has taught the microprocessor system of claim 11 in which the computation of said means for computing modifies the bus access time to provide sufficient time for input-output cycles ('471 column 3, line 37 to column 4, line 52; column 5, lines 43-59; and Figure 3; and '985 column 4, line 21 to column 5, line 25 and Figure 4).

27. Referring to claim 27, '471 and '985 have taught a microprocessor system, comprising

a. A microprocessing unit ('471 column 2, lines 4-45; column 2, line 57 to column 3, line 27; Figure 2A; and Figure 2B),

b. An input-output processor (IOP) ('471 column 2, lines 4-45; column 2, line 57 to column 3, line 27; Figure 2A; and Figure 2B), and

c. A memory interface unit selectively coupling said central processing unit and said IOP to a system bus ('471 column 3, lines 44-66). In regards to '471, the address decoder, which determines which memory address is being accessed by the CPU or IOP, is the memory interface.

d. Said IOP including program counter means for providing system address information to said memory interface unit ('471 column 3, lines 44-48 and Figure 3). In regards to '471, the memory address register is in communication with the rest of the CPU and holds the address of an instruction.

28. Referring to claim 28, '471 and '985 have taught the microprocessor system of claim 27 further including means, coupled to said IOP and to said system bus, for granting said IOP access to said system bus at predetermined intervals ('471 column 3, line 37 to column 4, line 52; column 5, lines 43-59; and Figure 3; and '985 column 4, line 21 to column 5, line 25 and Figure 4). In regards to '471, the focus of the discussion was on the bus arbitration and '985 discuses the timing of the accesses allowed to the bus.

29. Referring to claim 29, '471 and '985 have taught the microprocessor system of claim 27 wherein said IOP includes latch means, coupled to said system bus, for latching data received

from said system bus ('471 column 3, line 44 to column 4, line 19 and Figure 3). In regards '471, the ports latch data in response to an I/O command.

30. Referring to claim 30, '471 and '985 have taught the microprocessor system of claim 27 wherein said IOP includes a multiplexer controlled by said program counter means, an instruction latch, and a decode/execute module, said multiplexer coupled between said instruction latch and said decode/execute module ('471 column 3, line 44 to column 4, line 52 and Figure 3). In regards to '471, there are several port and multiplexer combinations in Figure 3 that meet this definition. For example, the memory address register 303 sends the address to selector 310, which decodes and identifies an I/O read operation from external memory. It then selects to send a signal to expansion port 318 to latch the address from memory address register 303.

Claim Rejections - 35 USC § 103

31. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

32. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Briggs et al., U.S. Patent Number 4,649,471 (herein referred to as '471) and U.S. Patent Number 4,626,985 (herein referred to as '985), which was incorporated by reference into '471 in column 3, lines 60-63, as applied to claim 1 above, and further in view of Niehaus et al., U.S. Patent Number 4,835,738 (herein referred to as Niehaus). '471 and '985 have not taught the microprocessor system of claim 1 wherein said central processing unit includes an arithmetic logic unit and a push-down

stack coupled to said arithmetic logic unit. Niehaus has taught wherein said central processing unit includes an arithmetic logic unit and a push-down stack coupled to said arithmetic logic unit (Niehaus column 1, lines 11-57; column 2, lines 44-59; column 4, lines 3-15 and 49-63; Figure 1; and Figure 2). A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught in Niehaus, that an ALU and register stack system, like that of Niehaus, allows for more designer customization to meet the designer's needs (Niehaus column 1, lines 12-14 and 23-25). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the ALU and stack of Niehaus in the device of '471 and '985 to improve customization.

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Glass, U.S. Patent Number 4,320,467, has taught a multi-processor system with a shared bus that requires arbitration.

b. Binder et al., U.S. Patent Number 4,488,217, has taught a multi-processor system with shared memory and a single, common bus that both require arbitration to share them.

c. Manton et al., U.S. Patent Number 4,509,115, has taught a system with a memory unit, central processing unit, and input/output unit.

d. Berger et al., U.S. Patent Number 4,679,166, has taught a dual processor with a designated I/O processor and an arbitrator between the two processors to shared memory.

e. Rehwald et al., U.S. Patent Number 4,760,521, has taught a multi-processor system with a main CPU, I/O system, and shared memory that respond to an arbitration system.

f. Sfarti et al., U.S. Patent Number 4,809,169, has taught a multi-processor system with bus arbitration between the processors.

g. Gulick, U.S. Patent Number 4,809,269, and Gullis et al., U.S. Patent Number 4,907,225, has taught a dual port timing controller that arbitrates access to shared memory.

h. Culler, U.S. Patent Number 4,837,682, has taught a clock cycle based bus arbitration system.

i. Gach et al., U.S. Patent Number 4,912,632 and EPO 0 288 649 A1, has taught a multi-processor system with shared memory.

j. Tulpule et al., U.S. Patent Number 4,959,782, has taught a multi-processor system with I/O arbitration.

k. Jamoun et al., U.S. Patent Number 4,967,398, has taught a control and arbitration device for memory and bus.

l. Kinter et al., U.S. Patent Number 5,047,921, has taught a time based arbitration system for shared memory.

m. Gillet, Jr. et al., U.S. Patent Number 5,068,781, has taught an arbiter for a shared bus and memory.

n. Boury et al., U.S. Patent Number 5,239,631, has taught a time based arbiter for CPU bus ownership.

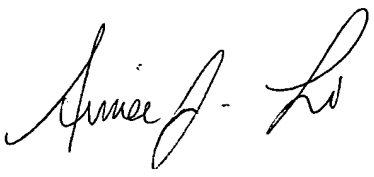
o. Cadambi et al., U.S. Patent Number 5,261,109, has taught arbitrating shared bus access to a multi-processor system with shared memory and an I/O processor.

p. Fuoco et al., U.S. Patent Number 5,353,417, has taught an arbitration method for a multi-processor system with I/O access.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

35. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

36. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



AJL
Aimee J. Li
09 December 2006